

CPLD 1 Specification

64 port G-PON

ASGvOLT64

(GPON OLT)

Version:1.0

Revision History

Document Rev.	Date	Author	Revision Description	CPLD code version
1.0	8/29/2019		Initial OCP Release	1.0

3.1. Offset 0x01 CPLD version (Read Only)

Example : version 5.01 then reg 0x1 is 5, reg 0x2 is 1

Bit	Name	R/W	Reset Value	Description
7:0	CPLD_ver[7:0]	R	1	CPLD version

3.2. Offset 0x02 CPLD version (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	CPLD_ver[7:0]	R	0	CPLD version

3.3. Offset 0x03 SFP_ABS_1 (Read Only)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 13	MPL1_SFP07_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
6	PON Port 12	MPL1_SFP06_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
5	PON Port 9	MPL1_SFP05_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
4	PON Port 8	MPL1_SFP04_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
3	PON Port 5	MPL1_SFP03_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
2	PON Port 4	MPL1_SFP02_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
1	PON Port 1	MPL1_SFP01_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
0	PON Port 0	MPL1_SFP00_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent

3.4. Offset 0x04 SFP_ABS_1 Mask (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 13	MASK*MPL1_SF P07_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
6	PON Port 12	MASK*MPL1_SF P06_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
5	PON Port 9	MASK*MPL1_SF P05_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
4	PON Port 8	MASK*MPL1_SF P04_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
3	PON Port 5	MASK*MPL1_SF P03_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
2	PON Port 4	MASK*MPL1_SF P02_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
1	PON Port 1	MASK*MPL1_SF P01_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
0	PON Port 0	MASK*MPL1_SF P00_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU

3.5. Offset 0x05 SFP_ABS_2 (Read Only)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 2	MPL1_SFP15_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
6	PON Port 3	MPL1_SFP14_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
5	PON Port 6	MPL1_SFP13_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
4	PON	MPL1_SFP12_MOD_ABS	R	1	0: SFP transceiver is present

	Port 7				1: SFP transceiver is absent
3	PON Port 10	MPL1_SFP11_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
2	PON Port 11	MPL1_SFP10_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
1	PON Port 14	MPL1_SFP09_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
0	PON Port 15	MPL1_SFP08_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent

3.6. Offset 0x06 SFP_ABS_2 Mask (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 2	MASK*MPL1_SF P15_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
6	PON Port 3	MASK*MPL1_SF P14_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
5	PON Port 6	MASK*MPL1_SF P13_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
4	PON Port 7	MASK*MPL1_SF P12_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
3	PON Port 10	MASK*MPL1_SF P11_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
2	PON Port 11	MASK*MPL1_SF P10_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
1	PON Port 14	MASK*MPL1_SF P09_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
0	PON Port 15	MASK*MPL1_SF P08_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU

3.7. Offset 0x07 SFP_ABS_3 (Read Only)

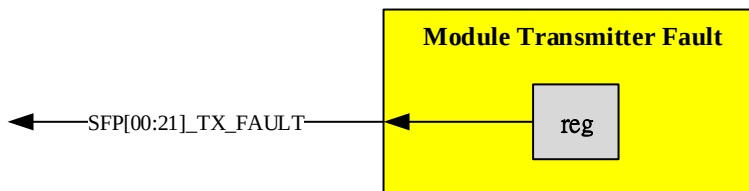
Bit	Front port	Name	R/W	Reset Value	Description
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7:6		Reserved			
5	PON Port 25	MPL2_SFP21_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
4	PON Port 24	MPL2_SFP20_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
3	PON Port 21	MPL2_SFP19_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
2	PON Port 20	MPL2_SFP18_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
1	PON Port 17	MPL2_SFP17_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent
0	PON Port 16	MPL2_SFP16_MOD_ABS	R	1	0: SFP transceiver is present 1: SFP transceiver is absent

3.8. Offset 0x08 SFP_ABS_3 Mask (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7:6		Reserved			
5	PON Port 25	MASK*MPL2_SF P21_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
4	PON Port 24	MASK*MPL2_SF P20_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
3	PON Port 21	MASK*MPL2_SF P19_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
2	PON Port 20	MASK*MPL2_SF P18_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
1	PON Port 17	MASK*MPL2_SF P17_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
0	PON Port 16	MASK*MPL2_SF P16_MOD_ABS	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU

3.9. Offset 0x09 SFP_TX_Fault_1 (Read only)



The module transmitter fault signal indicates transmitter has detected a fault condition related to laser operation or safety.

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 13	MPL1_SFP07_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
6	PON Port 12	MPL1_SFP06_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
5	PON Port 9	MPL1_SFP05_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
4	PON Port 8	MPL1_SFP04_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
3	PON Port 5	MPL1_SFP03_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
2	PON Port 4	MPL1_SFP02_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
1	PON Port 1	MPL1_SFP01_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
0	PON Port 0	MPL1_SFP00_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well

3.10. Offset 0x10 SFP_TX_Fault_1 Mask (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 13	MASK*MPL1_SF P07_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
6	PON	MASK*MPL1_SF	R/W	0	1: CPLD passes the Transmit Fault to CPU

	Port 12	P06_TX_FAULT			0: CPLD blocks incoming the Transmit Fault
5	PON Port 9	MASK*MPL1_SF P05_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
4	PON Port 8	MASK*MPL1_SF P04_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
3	PON Port 5	MASK*MPL1_SF P03_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
2	PON Port 4	MASK*MPL1_SF P02_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
1	PON Port 1	MASK*MPL1_SF P01_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
0	PON Port 0	MASK*MPL1_SF P00_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault

3.11. Offset 0x11 SFP_TX_Fault_2 (Read only)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 2	MPL1_SFP15_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
6	PON Port 3	MPL1_SFP14_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
5	PON Port 6	MPL1_SFP13_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
4	PON Port 7	MPL1_SFP12_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
3	PON Port 10	MPL1_SFP11_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
2	PON Port 11	MPL1_SFP10_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
1	PON Port 14	MPL1_SFP09_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
0	PON Port 15	MPL1_SFP08_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well

3.12. Offset 0x12 SFP_TX_Fault_2 Mask (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	MASK*MPL1_SFP15_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
6	MASK*MPL1_SFP14_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
5	MASK*MPL1_SFP13_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
4	MASK*MPL1_SFP12_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
3	MASK*MPL1_SFP11_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
2	MASK*MPL1_SFP10_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
1	MASK*MPL1_SFP09_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
0	MASK*MPL1_SFP08_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault

3.13. Offset 0x13 SFP_TX_Fault_3 (Read only)

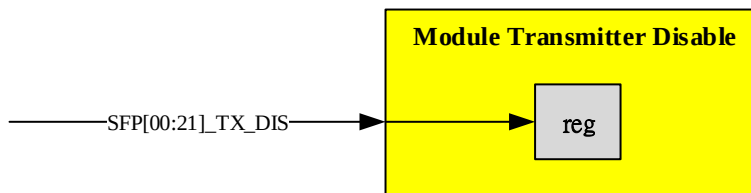
Bit	Front port	Name	R/W	Reset Value	Description
7:6		Reserved			
5	PON Port 25	MPL2_SFP21_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
4	PON Port 24	MPL2_SFP20_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
3	PON Port 21	MPL2_SFP19_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working

					well
2	PON Port 20	MPL2_SFP18_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
1	PON Port 17	MPL2_SFP17_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well
0	PON Port 16	MPL2_SFP16_TX_FAULT	R	1	1: SFP Transmit Fault 0: SFP Transmitter is working well

3.14. Offset 0x14 SFP_TX_Fault_3 Mask (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7:6		Reserved			
5	PON Port 25	MASK*MPL2_SF P21_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
4	PON Port 24	MASK*MPL2_SF P20_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
3	PON Port 21	MASK*MPL2_SF P19_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
2	PON Port 20	MASK*MPL2_SF P18_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
1	PON Port 17	MASK*MPL2_SF P17_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault
0	PON Port 16	MASK*MPL2_SF P16_TX_FAULT	R/W	0	1: CPLD passes the Transmit Fault to CPU 0: CPLD blocks incoming the Transmit Fault

3.15. Offset 0x15 SFP_TX_Disable_1 (Read& Write)



The module transmitter disable signal indicates transmitter's output is turned off or not. It is independent of the data inputs.

Bit	Front port	Net Name	R/W	Reset Value	Description
7	PON Port 13	MPL1_SFP07_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
6	PON Port 12	MPL1_SFP06_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
5	PON Port 9	MPL1_SFP05_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
4	PON Port 8	MPL1_SFP04_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
3	PON Port 5	MPL1_SFP03_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
2	PON Port 4	MPL1_SFP02_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
1	PON Port 1	MPL1_SFP01_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
0	PON Port 0	MPL1_SFP00_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off

3.16. Offset 0x16 SFP_TX_Disable_1 Mask (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 13	MASK*MPL1_SFP07_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.

6	PON Port 12	MASK*MPL1_SFP06_TX _DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
5	PON Port 9	MASK*MPL1_SFP05_TX _DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
4	PON Port 8	MASK*MPL1_SFP04_TX _DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
3	PON Port 5	MASK*MPL1_SFP03_TX _DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
2	PON Port 4	MASK*MPL1_SFP02_TX _DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
1	PON Port 1	MASK*MPL1_SFP01_TX _DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
0	PON Port 0	MASK*MPL1_SFP00_TX _DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.

3.17. Offset 0x17 SFP_TX_Disable_2 (Read& Write)

Bit	Front port	Net Name	R/W	Reset Value	Description
7	PON Port 2	MPL1_SFP15_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
6	PON Port 3	MPL1_SFP14_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
5	PON Port 6	MPL1_SFP13_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
4	PON Port 7	MPL1_SFP12_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
3	PON Port 10	MPL1_SFP11_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
2	PON Port 11	MPL1_SFP10_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
1	PON Port 14	MPL1_SFP09_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off

0	PON Port 15	MPL1_SFP08_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
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3.18. Offset 0x18 SFP_TX_Disable_2 Mask (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 2	MASK*MPL1_SFP15_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
6	PON Port 3	MASK*MPL1_SFP14_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
5	PON Port 6	MASK*MPL1_SFP13_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
4	PON Port 7	MASK*MPL1_SFP12_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
3	PON Port 10	MASK*MPL1_SFP11_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
2	PON Port 11	MASK*MPL1_SFP10_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
1	PON Port 14	MASK*MPL1_SFP09_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
0	PON Port 15	MASK*MPL1_SFP08_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.

3.19. Offset 0x19 SFP_TX_Disable_3 (Read& Write)

Bit	Front port	Net Name	R/W	Reset Value	Description
7:6		Reserved			
5	PON Port 25	MPL2_SFP21_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
4	PON Port 24	MPL2_SFP20_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
3	PON	MPL2_SFP19_TX_DIS	R/W	1	0: Transmitter output is turned on

	Port 21				1: Transmitter output is turned off
2	PON Port 20	MPL2_SFP18_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
1	PON Port 17	MPL2_SFP17_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off
0	PON Port 16	MPL2_SFP16_TX_DIS	R/W	1	0: Transmitter output is turned on 1: Transmitter output is turned off

3.20. Offset 0x20 SFP_TX_Disable_3 Mask (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7:6		Reserved			
5	PON Port 25	MASK*MPL2_SFP21_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
4	PON Port 24	MASK*MPL2_SFP20_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
3	PON Port 21	MASK*MPL2_SFP19_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
2	PON Port 20	MASK*MPL2_SFP18_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
1	PON Port 17	MASK*MPL2_SFP17_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.
0	PON Port 16	MASK*MPL2_SFP16_TX_DIS	R/W	1	1: CPLD can control the TX disable. 0: CPLD cannot control the TX disable.

3.21. Offset 0x21 SFP_LED_ACT (Read& Write)

Will remove at next version

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 13	SFP07_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON

6	PON Port 12	SFP06_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
5	PON Port 9	SFP05_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
4	PON Port 8	SFP04_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
3	PON Port 5	SFP03_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
2	PON Port 4	SFP02_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
1	PON Port 1	SFP01_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
0	PON Port 0	SFP00_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON

3.22. Offset 0x22 SFP_LED_ACT (Read& Write)

Will remove at next version

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 2	SFP15_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
6	PON Port 3	SFP14_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
5	PON Port 6	SFP13_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
4	PON Port 7	SFP12_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
3	PON Port 10	SFP11_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
2	PON Port 11	SFP10_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
1	PON	SFP09_LED_ACT	W	1	Steady: No traffic

	Port 14				Blinking: Indicates data traffic on the PON
0	PON Port 15	SFP08_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON

3.23. Offset 0x23 SFP_LED_ACT (Read& Write)

Will remove at next version

Bit	Front port	Name	R/W	Reset Value	Description
7:6		Reserved			
5	PON Port 25	SFP21_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
4	PON Port 24	SFP20_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
3	PON Port 21	SFP19_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
2	PON Port 20	SFP18_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
1	PON Port 17	SFP17_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON
0	PON Port 16	SFP16_LED_ACT	W	1	Steady: No traffic Blinking: Indicates data traffic on the PON

3.24. Offset 0x24 GPON SFP_LED_LINK_G (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 13	SFP07_LED_LINK_G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
6	PON Port 12	SFP06_LED_LINK_G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
5	PON Port 9	SFP05_LED_LINK_G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service

4	PON Port 8	SFP04_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
3	PON Port 5	SFP03_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
2	PON Port 4	SFP02_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
1	PON Port 1	SFP01_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
0	PON Port 0	SFP00_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service

3.25. Offset 0x25 GPON SFP_LED_LINK_G (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 2	SFP15_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
6	PON Port 3	SFP14_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
5	PON Port 6	SFP13_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
4	PON Port 7	SFP12_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
3	PON Port 10	SFP11_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
2	PON Port 11	SFP10_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
1	PON Port 14	SFP09_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
0	PON Port 15	SFP08_LED_LINK _G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service

3.26. Offset 0x26 GPON SFP_LED_LINK_G (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7:6		Reserved			
5	PON Port 25	SFP21_LED_LINK_G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
4	PON Port 24	SFP20_LED_LINK_G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
3	PON Port 21	SFP19_LED_LINK_G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
2	PON Port 20	SFP18_LED_LINK_G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
1	PON Port 17	SFP17_LED_LINK_G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service
0	PON Port 16	SFP16_LED_LINK_G	R/W	1	0: PON link up & 1 or more ONTs in service 1: No ONT in service

3.27. Offset 0x27 GPON SFP_LED_LINK_B (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 13	SFP07_LED_LINK_B	R/W	1	0: Port disabled 1: Port enabled
6	PON Port 12	SFP06_LED_LINK_B	R/W	1	0: Port disabled 1: Port enabled
5	PON Port 9	SFP05_LED_LINK_B	R/W	1	0: Port disabled 1: Port enabled
4	PON Port 8	SFP04_LED_LINK_B	R/W	1	0: Port disabled 1: Port enabled
3	PON Port 5	SFP03_LED_LINK_B	R/W	1	0: Port disabled 1: Port enabled
2	PON Port 4	SFP02_LED_LINK_B	R/W	1	0: Port disabled 1: Port enabled

1	PON Port 1	SFP01_LED_LINK _B	R/W	1	0: Port disabled 1: Port enabled
0	PON Port 0	SFP00_LED_LINK _B	R/W	1	0: Port disabled 1: Port enabled

3.28. Offset 0x28 GPON SFP_LED_LINK_B (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 2	SFP15_LED_LINK _B	R/W	1	0: Port disabled 1: Port enabled
6	PON Port 3	SFP14_LED_LINK _B	R/W	1	0: Port disabled 1: Port enabled
5	PON Port 6	SFP13_LED_LINK _B	R/W	1	0: Port disabled 1: Port enabled
4	PON Port 7	SFP12_LED_LINK _B	R/W	1	0: Port disabled 1: Port enabled
3	PON Port 10	SFP11_LED_LINK _B	R/W	1	0: Port disabled 1: Port enabled
2	PON Port 11	SFP10_LED_LINK _B	R/W	1	0: Port disabled 1: Port enabled
1	PON Port 14	SFP09_LED_LINK _B	R/W	1	0: Port disabled 1: Port enabled
0	PON Port 15	SFP08_LED_LINK _B	R/W	1	0: Port disabled 1: Port enabled

3.29. Offset 0x29 GPON SFP_LED_LINK_B (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7:6		Reserved			
5	PON Port 25	SFP21_LED_LINK _B	R/W	1	0: Port disabled 1: Port enabled
4	PON Port 24	SFP20_LED_LINK _B	R/W	1	0: Port disabled 1: Port enabled

3	PON Port 21	SFP19_LED_LINK _B	R/W	1	0: Port disabled 1: Port enabled
2	PON Port 20	SFP18_LED_LINK _B	R/W	1	0: Port disabled 1: Port enabled
1	PON Port 17	SFP17_LED_LINK _B	R/W	1	0: Port disabled 1: Port enabled
0	PON Port 16	SFP16_LED_LINK _B	R/W	1	0: Port disabled 1: Port enabled

3.30. Offset 0x30 GPON SFP_LED_LINK_R (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON Port 13	SFP07_LED_LINK _R	R/W	1	0: Fault detected 1: Normal operation
6	PON Port 12	SFP06_LED_LINK _R	R/W	1	0: Fault detected 1: Normal operation
5	PON Port 9	SFP05_LED_LINK _R	R/W	1	0: Fault detected 1: Normal operation
4	PON Port 8	SFP04_LED_LINK _R	R/W	1	0: Fault detected 1: Normal operation
3	PON Port 5	SFP03_LED_LINK _R	R/W	1	0: Fault detected 1: Normal operation
2	PON Port 4	SFP02_LED_LINK _R	R/W	1	0: Fault detected 1: Normal operation
1	PON Port 1	SFP01_LED_LINK _R	R/W	1	0: Fault detected 1: Normal operation
0	PON Port 0	SFP00_LED_LINK _R	R/W	1	0: Fault detected 1: Normal operation

3.31. Offset 0x31 GPON SFP_LED_LINK_R (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7	PON	SFP15_LED_LINK	R/W	1	0: Fault detected

	Port 2	_R			1: Normal operation
6	PON Port 3	SFP14_LED_LINK _R	R/W	1	0: Fault detected 1: Normal operation
5	PON Port 6	SFP13_LED_LINK _R	R/W	1	0: Fault detected 1: Normal operation
4	PON Port 7	SFP12_LED_LINK _R	R/W	1	0: Fault detected 1: Normal operation
3	PON Port 10	SFP11_LED_LINK _R	R/W	1	0: Fault detected 1: Normal operation
2	PON Port 11	SFP10_LED_LINK _R	R/W	1	0: Fault detected 1: Normal operation
1	PON Port 14	SFP09_LED_LINK _R	R/W	1	0: Fault detected 1: Normal operation
0	PON Port 15	SFP08_LED_LINK _R	R/W	1	0: Fault detected 1: Normal operation

3.32. Offset 0x32 GPON SFP_LED_LINK_R (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7:6		Reserved			
5	PON Port 25	SFP21_LED_LINK _R	R/W	1	0: Fault detected 1: Normal operation
4	PON Port 24	SFP20_LED_LINK _R	R/W	1	0: Fault detected 1: Normal operation
3	PON Port 21	SFP19_LED_LINK _R	R/W	1	0: Fault detected 1: Normal operation
2	PON Port 20	SFP18_LED_LINK _R	R/W	1	0: Fault detected 1: Normal operation
1	PON Port 17	SFP17_LED_LINK _R	R/W	1	0: Fault detected 1: Normal operation
0	PON Port 16	SFP16_LED_LINK _R	R/W	1	0: Fault detected 1: Normal operation

3.33. Offset 0x33 QSFP28 MOD (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7:2		Reserved			
1	100G Port 1	QSFP28_MODE_P1	R/W	1	0: Set LPMODE in High Power. 1: Set LPMODE in Lowe Power.
0	100G Port 0	QSFP28_MODE_P0	R/W	1	0: Set LPMODE in High Power. 1: Set LPMODE in Lowe Power.

3.34. Offset 0x34 QSFP28 PRSNT (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7:2		Reserved			
1	100G Port 1	QSFP28_PRSNT_P1	R	1	0: Show QSFP28 module has been installed 1: No QSFP+ module be installed
0	100G Port 0	QSFP28_PRSNT_P0	R	1	0: Show QSFP28 module has been installed 1: No QSFP+ module be installed

3.35. Offset 0x35 QSFP28_LED_LINK_G (Read& Write)

Will remove at next version

Bit	Front port	Name	R/W	Reset Value	Description
7	100G Port 1	QSFP28_P1_LAN E3_LED_LINK_G	W	1	0: Link up (speed 25G) 1: Link down Blinking: Indicates data traffic on the PON
6	100G Port 1	QSFP28_P1_LAN E2_LED_LINK_G	W	1	0: Link up (speed 25G) 1: Link down Blinking: Indicates data traffic on the PON
5	100G Port 1	QSFP28_P1_LAN E1_LED_LINK_G	W	1	0: Link up (speed 25G) 1: Link down

					Blinking: Indicates data traffic on the PON
4	100G Port 1	QSFP28_P1_LAN E0_LED_LINK_G	W	1	0: Link up (speed 25G) 1: Link down Blinking: Indicates data traffic on the PON
3	100G Port 0	QSFP28_P0_LAN E3_LED_LINK_G	W	1	0: Link up (speed 25G) 1: Link down Blinking: Indicates data traffic on the PON
2	100G Port 0	QSFP28_P0_LAN E2_LED_LINK_G	W	1	0: Link up (speed 25G) 1: Link down Blinking: Indicates data traffic on the PON
1	100G Port 0	QSFP28_P0_LAN E1_LED_LINK_G	W	1	0: Link up (speed 25G) 1: Link down Blinking: Indicates data traffic on the PON
0	100G Port 0	QSFP28_P0_LAN E0_LED_LINK_G	W	1	0: Link up (speed 25G) 1: Link down Blinking: Indicates data traffic on the PON

3.36. Offset 0x36 QSFP28_LED_LINK_B (Read& Write)

Will remove at next version

Bit	Front port	Name	R/W	Reset Value	Description
7	100G Port 1	QSFP28_P1_LAN E3_LED_LINK_B	W	1	0: Link up (speed 10G) 1: Link down Blinking: Indicates data traffic on the PON
6	100G Port 1	QSFP28_P1_LAN E2_LED_LINK_B	W	1	0: Link up (speed 10G) 1: Link down Blinking: Indicates data traffic on the PON
5	100G Port 1	QSFP28_P1_LAN E1_LED_LINK_B	W	1	0: Link up (speed 10G) 1: Link down Blinking: Indicates data traffic on the PON
4	100G Port 1	QSFP28_P1_LAN E0_LED_LINK_B	W	1	0: Link up (speed 10G) 1: Link down

					Blinking: Indicates data traffic on the PON
3	100G Port 0	QSFP28_P0_LAN E3_LED_LINK_B	W	1	0: Link up (speed 10G) 1: Link down Blinking: Indicates data traffic on the PON
2	100G Port 0	QSFP28_P0_LAN E2_LED_LINK_B	W	1	0: Link up (speed 10G) 1: Link down Blinking: Indicates data traffic on the PON
1	100G Port 0	QSFP28_P0_LAN E1_LED_LINK_B	W	1	0: Link up (speed 10G) 1: Link down Blinking: Indicates data traffic on the PON
0	100G Port 0	QSFP28_P0_LAN E0_LED_LINK_B	W	1	0: Link up (speed 10G) 1: Link down Blinking: Indicates data traffic on the PON

3.37. Offset 0x37 QSFP28_LED_LINK_O (Read& Write)

Will remove at next version

Bit	Front port	Name	R/W	Reset Value	Description
7	100G Port 1	QSFP28_P1_LAN E3_LED_LINK_O	W	1	0: Link up (speed 1G) 1: Link down Blinking: Indicates data traffic on the PON
6	100G Port 1	QSFP28_P1_LAN E2_LED_LINK_O	W	1	0: Link up (speed 1G) 1: Link down Blinking: Indicates data traffic on the PON
5	100G Port 1	QSFP28_P1_LAN E1_LED_LINK_O	W	1	0: Link up (speed 1G) 1: Link down Blinking: Indicates data traffic on the PON
4	100G Port 1	QSFP28_P1_LAN E0_LED_LINK_O	W	1	0: Link up (speed 1G) 1: Link down Blinking: Indicates data traffic on the PON

3	100G Port 0	QSFP28_P0_LAN E3_LED_LINK_O	W	1	0: Link up (speed 1G) 1: Link down Blinking: Indicates data traffic on the PON
2	100G Port 0	QSFP28_P0_LAN E2_LED_LINK_O	W	1	0: Link up (speed 1G) 1: Link down Blinking: Indicates data traffic on the PON
1	100G Port 0	QSFP28_P0_LAN E1_LED_LINK_O	W	1	0: Link up (speed 1G) 1: Link down Blinking: Indicates data traffic on the PON
0	100G Port 0	QSFP28_P0_LAN E0_LED_LINK_O	W	1	0: Link up (speed 1G) 1: Link down Blinking: Indicates data traffic on the PON

3.38. Offset 0x38 Reserve (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	Reserved			
6	CPLD1_FPGA1_RESERVE_E	R/W	1	Reserve from CPLD1 to FPGA1
5	CPLD1_FPGA1_RESERVE_D	R/W	1	Reserve from CPLD1 to FPGA1
4	FPGA1_CPLD1_RESERVE_A	R/W	1	Reserve from FPGA1 to CPLD1
3	CPLD3_CPLD1_RESERVE_A	R/W	1	Reserve from CPLD3 to CPLD1
2	CPLD2_CPLD1_RESERVE_C	R/W	1	Reserve from CPLD2 to CPLD1
1	CPLD2_CPLD1_RESERVE_B	R/W	1	Reserve from CPLD2 to CPLD1
0	CPLD2_CPLD1_RESERVE_A	R/W	1	Reserve from CPLD2 to CPLD1

3.39. Offset 0x39 CPU I2C (Read& Write)

Will remove at next version

Bit	Name	R/W	Reset Value	Description
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7:4	Reserved			
1	CPLD_1_CPU_SDA	R/W		SDA from CPU to CPLD1
0	CPLD_1_CPU_SCL	R/W		SCL from CPU to CPLD1

3.40. Offset 0x40 LED Stream (Read& Write)

Will remove at next version

Bit	Name	R/W	Reset Value	Description
7:4	Reserved			
3	CPLD1_PON_LED_DATA	R/W		PON LED DATA from FPGA2 to CPLD1
2	CPLD1_PON_LED_CLK	R/W		PON LED CLK from FPGA2 to CPLD1
1	CPLD1_UPLINK_LED_DATA	R/W		Uplink LED DATA from FPGA2 to CPLD1
0	CPLD1_UPLINK_LED_CLK	R/W		Uplink LED CLK from FPGA2 to CPLD1

4.1. Offset 0x01 Power Enable (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	System Power down/up	R/W	1	0: System Power down 1: System Power up
6	USB_VCC5P0_Enable	R/W	1	1: Enable. 0: Disable
5	FAN_CPLD_3V3_ENABLE	R/W	1	1: Enable. 0: Disable
4	BMC_5V0_ENABLE	R/W	1	1: Enable. 0: Disable
3	12V_FAN_Power_EN	R/W	1	1: Enable the Hot swap for FAN board. 0: Reset the Hot swap for FAN board.
2	12V_BMC_Power_EN	R/W	1	1: Enable the Hot swap for BMC board. 0: Reset the Hot swap for BMC board.
1	Reserved			
0	Reserved			

4.2. Offset 0x02 Reset Output (Read& Write)

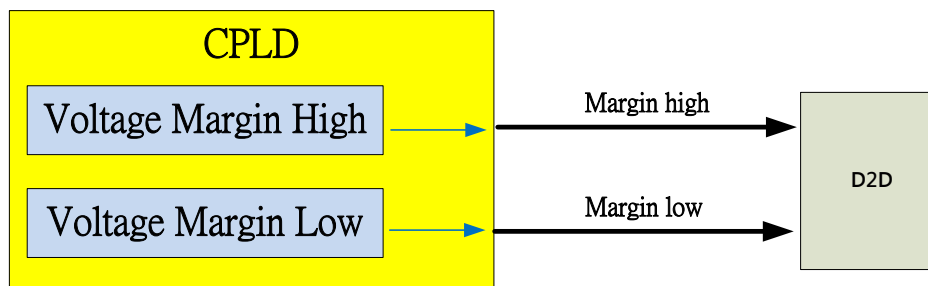
Bit	Name	R/W	Reset Value	Description
7:1	Reserved			
0	FPGA2_SPI_RST_N	R/W	1	1: Normal status. 0: Reset FPGA2 SPI flash by SW.

4.3. Offset 0x03 Power present (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:1	Reserved			
0	MAIN_BOARD_POWER_PRESENT_3	R/W	0	0: Main board power off 1: Main board power on

4.4. Offset 0x04 Voltage margin_1 (Read& Write)

TBD



Below table describes the voltage margining:

Vxx_High	Vxx_Low	Margin	Remarks
0	0	Margin_Low	
0	1	Nominal	
1	0	Nominal	Not used
1	1	Margin_High	

Bit	Name	R/W	Reset Value	Description
7	MPL_1V8_MARGIN_LOW	R/W	1	Enable Margin MPL_1V8
6	MPL_1V8_MARGIN_HIGH	R/W	0	Enable Margin MPL_1V8
5	MPL_1V5_R_MARGIN_LOW	R/W	1	Enable Margin MPL_1V5_R
4	MPL_1V5_R_MARGIN_HIGH	R/W	0	Enable Margin MPL_1V5_R
3	MPL_1V5_L_MARGIN_LOW	R/W	1	Enable Margin MPL_1V5_L
2	MPL_1V5_L_MARGIN_HIGH	R/W	0	Enable Margin MPL_1V5_L
1	FPGA_1V2_MARGIN_LOW	R/W	1	Enable Margin FPGA_1V2
0	FPGA_1V2_MARGIN_HIGH	R/W	0	Enable Margin FPGA_1V2

4.5. Offset 0x05 Voltage margin_2 (Read& Write)

TBD

Bit	Name	R/W	Reset Value	Description
7	VDD1P2_DDR_MARGIN_LOW	R/W	1	Enable Margin VDD1P2_DDR

6	VDD1P2_DDR_MARGIN_HIGH	R/W	0	Enable Margin VDD1P2_DDR
5	VDD1P0_MARGIN_LOW	R/W	1	Enable Margin VDD1P0
4	VDD1P0_MARGIN_HIGH	R/W	0	Enable Margin VDD1P0
3	MPL_R_1V_MARGIN_LOW	R/W	1	Enable Margin MPL_R_1V
2	MPL_R_1V_MARGIN_HIGH	R/W	0	Enable Margin MPL_R_1V
1	MPL_L_1V_MARGIN_LOW	R/W	1	Enable Margin MPL_L_1V
0	MPL_L_1V_MARGIN_HIGH	R/W	0	Enable Margin MPL_L_1V

4.6. Offset 0x06 Voltage margin_3 (Read& Write)

TBD

Bit	Name	R/W	Reset Value	Description
7:6	Reserved			
5	VPP_DDR2P5_MARGIN_LOW	R/W	1	Enable Margin VPP_DDR2P5
4	VPP_DDR2P5_MARGIN_HIGH	R/W	0	Enable Margin VPP_DDR2P5
3	VDD1P8_MARGIN_LOW	R/W	1	Enable Margin VDD1P8
2	VDD1P8_MARGIN_HIGH	R/W	0	Enable Margin VDD1P8
1	VDD1P25_MARGIN_LOW	R/W	1	Enable Margin VDD1P25
0	VDD1P25_MARGIN_HIGH	R/W	0	Enable Margin VDD1P25

4.7. Offset 0x07 Power present (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:1	Reserved			
0	Reserved			

4.8. Offset 0x08 QSFP28 RST (Read& Write)

Bit	Front port	Name	R/W	Reset Value	Description
7:2		Reserved			
1	100G Port 1	QSFP28_RST_P1_N	R/W	1	1: Normal status. 0: Reset QSFP28 Module

0	100G Port 0	QSFP28_RST_P0_N	R/W	1	1: Normal status. 0: Reset QSFP28 Module
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4.9. Offset 0x09 QSFP28 INT (Read only)

Bit	Front port	Name	R/W	Reset Value	Description
7:2		Reserved			
1	100G Port 1	QSFP28_INT_P1	R	1	0: Show module fault or status critical to system. 1: No interrupt
0	100G Port 0	QSFP28_INT_P0	R	1	0: Show module fault or status critical to system. 1: No interrupt

4.10. Offset 0x10 QSFP28 INT Mask (Read& Write)

(TBD)

Bit	Front port	Name	R/W	Reset Value	Description
7:2		Reserved			
1	100G Port 1	MASK*QSFP28_INT_P1	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
0	100G Port 0	MASK*QSFP28_INT_P0	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU

4.11. Offset 0x11 Reset Input (Read& Write)

(TBD)

Bit	Name	R/W	Reset Value	Description
7:1	Reserved			
0	CPLD3_TO_CPLD1_RESET	R/W	0	0: Normal operation 1: Reset CPLD1 by SW

4.12. Offset 0x12 Thermal Shut down (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:1	Reserved			
0	THERMAL_SHUT_DOWN_FPGA_OUTPUT	R/W	0	0: Normal operation 1: Thermal shut down signal from FPGA1

4.13. Offset 0x13 **TBD** (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:1	Reserved			
0	UCD9090_ALERT_L	R/W	0	

4.14. Offset 0x14 BMC I2C (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:4	Reserved			
1	CPLD_1_BMC_SDA	R/W		SDA from BMC to CPLD1
0	CPLD_1_BMC_SCL	R/W		SCL from BMC to CPLD1

4.15. Offset 0x15 Interrupt Stream (Read& Write)

(TBD)

Bit	Name	R/W	Reset Value	Description
7:4	Reserved			
1	CPLD1_TO_FPGA2_INTERRUPT_DATA	R/W		Interrupt DATA from CPLD1 to FPGA2
0	CPLD1_TO_FPGA2_INTERRUPT_CLK	R/W		Interrupt CLK from CPLD1 to FPGA2